

In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1 - 35. (Canceled)

36. (Original) A pFET synapse transistor, comprising:

- a p- doped substrate;
- a first n- well and a second n- well disposed in said substrate;
- a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;
- a channel disposed in said first n- well between said source and said drain;
- a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ region and said fourth p+ region together forming a tunneling junction;
- a layer of gate oxide disposed above said channel, said first n- well and said second n- well;
- a polysilicon floating gate disposed above said layer of gate oxide;
- a source contact terminal electrically coupled to said source;
- a drain contact terminal electrically coupled to said drain; and
- a well contact terminal electrically coupled to said second n- well.

37. (Original) A pFET synapse transistor in accordance with claim 36, wherein said third p+ doped region and said fourth p+ doped region are shorted together with a conductive layer which forms a bridge over said floating gate.

38. (Original) A pFET synapse transistor in accordance with claim 37, wherein said well contact terminal is strapped to said third p+ doped region and said fourth p+ doped region.

39. (Original) A pFET synapse transistor in accordance with claim 38, wherein said transistor is formed with a single layer of conductive polysilicon.

40. (Original) A pFET synapse transistor in accordance with claim 36 fabricated using a standard CMOS process.

41-43. (Canceled)

44. (Previously presented) A pFET synapse transistor, comprising:
a p- doped substrate;
a first n- well and a second n- well disposed in said substrate;
a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;
a channel disposed in said first n- well between said source and said drain;
a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ region and said fourth p+ region together forming a tunneling junction;
a layer of gate oxide disposed above said channel, said first n- well and said second n-

well;

a polysilicon floating gate disposed above said layer of gate oxide;
a source contact terminal electrically coupled to said source;
a drain contact terminal electrically coupled to said drain; and
a well contact terminal electrically coupled to said second n- well,
wherein said synapse transistor is configured to operate as a current source without gate
input using a single polysilicon gate layer.

45. (Previously presented) A system on a chip (SOC) including digital and analog
circuits integrated on a single semiconductor chip, the system comprising:

a pFET synapse transistor including:
a p- doped substrate;
a first n- well and a second n- well disposed in said substrate;
a first p+ doped region disposed in said first n- well forming a source and a
second p+ doped region disposed in said first n- well forming a drain;
a channel disposed in said first n- well between said source and said drain;
a third p+ doped region and a fourth p+ doped region disposed in said second n-
well, said third p+ region and said fourth p+ region together forming a tunneling junction;
a layer of gate oxide disposed above said channel, said first n- well and said
second n- well;
a polysilicon floating gate disposed above said layer of gate oxide;
a source contact terminal electrically coupled to said source;
a drain contact terminal electrically coupled to said drain; and
a well contact terminal electrically coupled to said second n- well.

46. (Previously presented) A p-channel floating-gate device, comprising:

- a p- doped substrate;
- a first n- well and a second n- well disposed in said substrate;
- a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;
- a channel disposed in said first n- well between said source and said drain;
- a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ region and said fourth p+ region together forming a tunneling junction;
- a layer of gate oxide disposed above said channel, said first n- well and said second n- well;
- a single polysilicon layer disposed above said layer of gate oxide, said single polysilicon layer comprising a floating gate;
- a source contact terminal electrically coupled to said source;
- a drain contact terminal electrically coupled to said drain; and
- a well contact terminal electrically coupled to said second n- well.

47. (Previously presented) A system on a chip (SOC) including digital and analog circuits integrated on a single semiconductor chip, the system comprising:

- a p-channel floating-gate device, including:
- a p- doped substrate;
- a first n- well and a second n- well disposed in said substrate;
- a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;

a channel disposed in said first n- well between said source and said drain;
a third p+ doped region and a fourth p+ doped region disposed in said second n- well,
said third p+ region and said fourth p+ region together forming a tunneling junction;
a layer of gate oxide disposed above said channel, said first n- well and said second n- well;
a single polysilicon layer disposed above said layer of gate oxide, said single polysilicon layer comprising a floating gate;
a source contact terminal electrically coupled to said source;
a drain contact terminal electrically coupled to said drain; and
a well contact terminal electrically coupled to said second n- well.

48. (Previously presented) A p-channel floating gate device comprising:

a p- doped substrate;
a first n- well and a second n- well disposed in said substrate;
a first p+ doped region disposed in said first n- well forming a source and a second p+ doped region disposed in said first n- well forming a drain;
a channel disposed in said first n- well between said source and said drain;
a third p+ doped region and a fourth p+ doped region disposed in said second n- well,
said third p+ region and said fourth p+ region together forming a tunneling junction;
a layer of gate oxide disposed above said channel, said first n- well and said second n- well;
a polysilicon floating gate disposed above said layer of gate oxide;
a source contact terminal electrically coupled to said source;
a drain contact terminal electrically coupled to said drain; and

a well contact terminal electrically coupled to said second n- well.

49. (Previously presented) A p-channel floating gate device in accordance with claim 48, wherein said third p+ doped region and said fourth p+ doped region are shorted together with a conductive layer which forms a bridge over said floating gate.

50. (Previously presented) A p-channel floating gate device in accordance with claim 49, wherein said well contact terminal is strapped to said third p+ doped region and said fourth p+ doped region.

51. (Previously presented) A p-channel floating gate device in accordance with claim 50, wherein said transistor is formed with a single layer of conductive polysilicon.

52. (Previously presented) A p-channel floating gate device in accordance with claim 48 fabricated using a standard CMOS process.